

**CACHE MEMORY ARCHITECTURE AND ASSOCIATED
MICROPROCESSOR DESIGN**

Taylor, et. al.,

Appl. No.: UNKNOWN Atty Docket: DATUMTE.015A

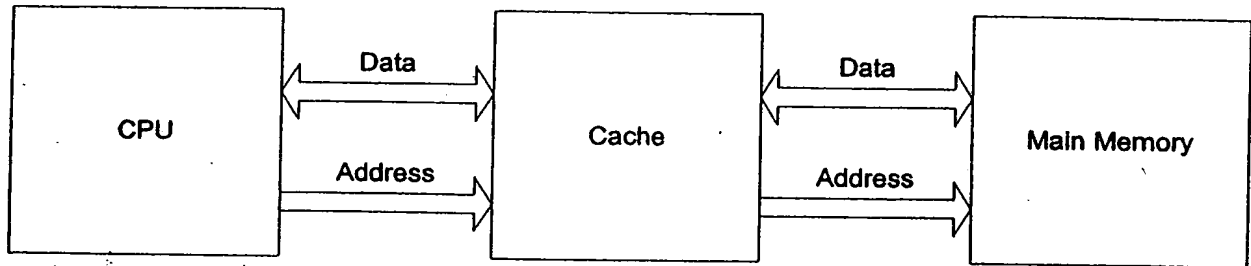


Figure 1.

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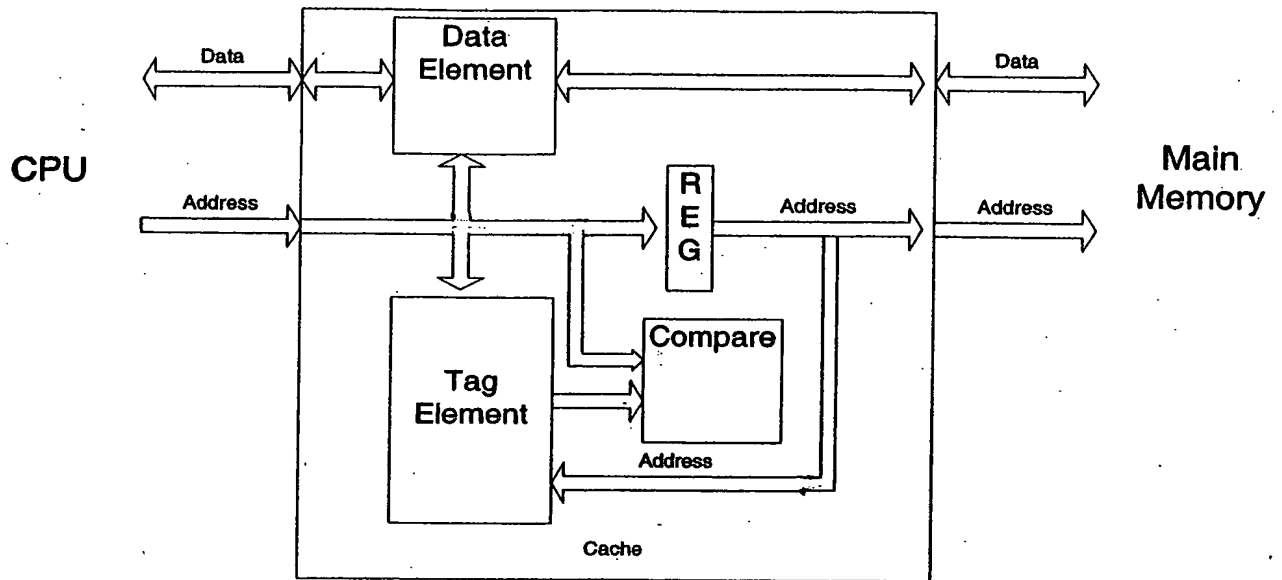


Figure 2.

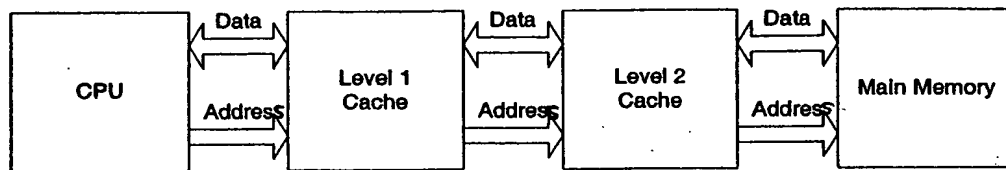


Figure 3.

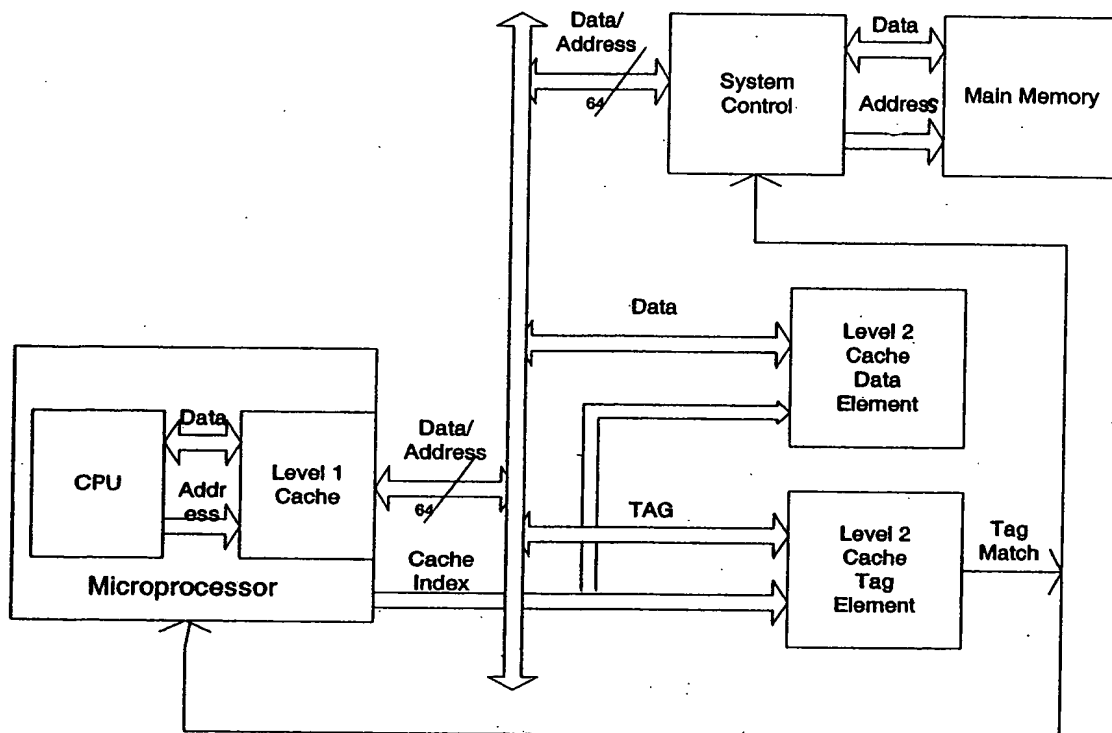


Figure 4.

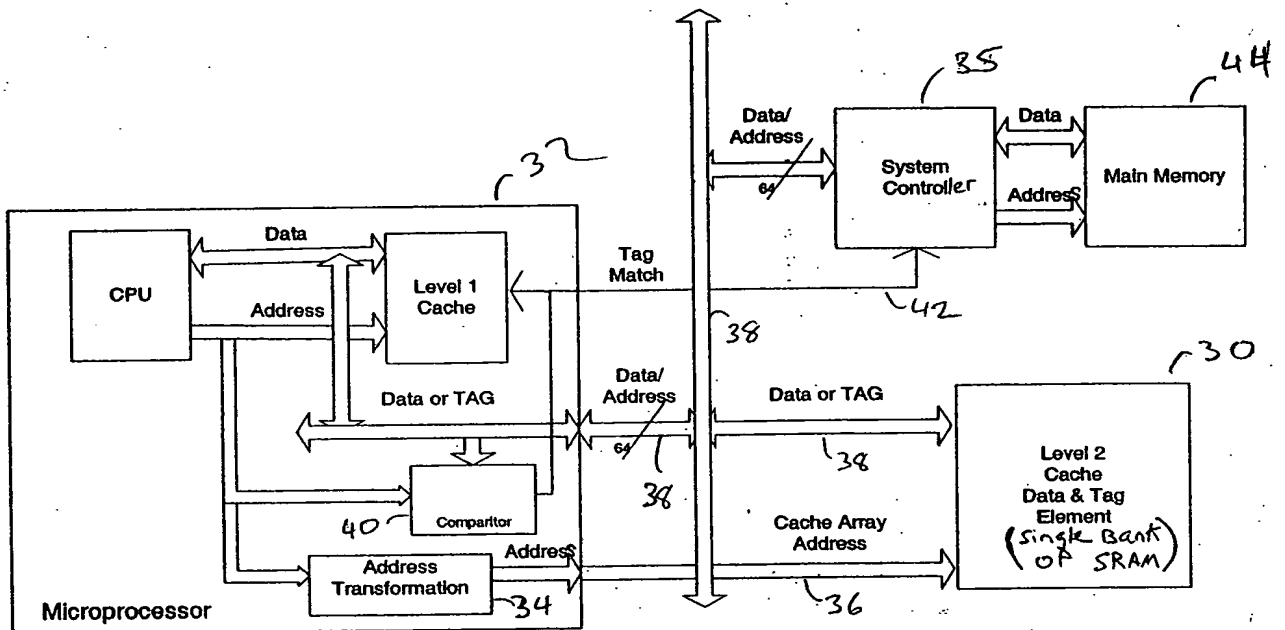


Figure 5.

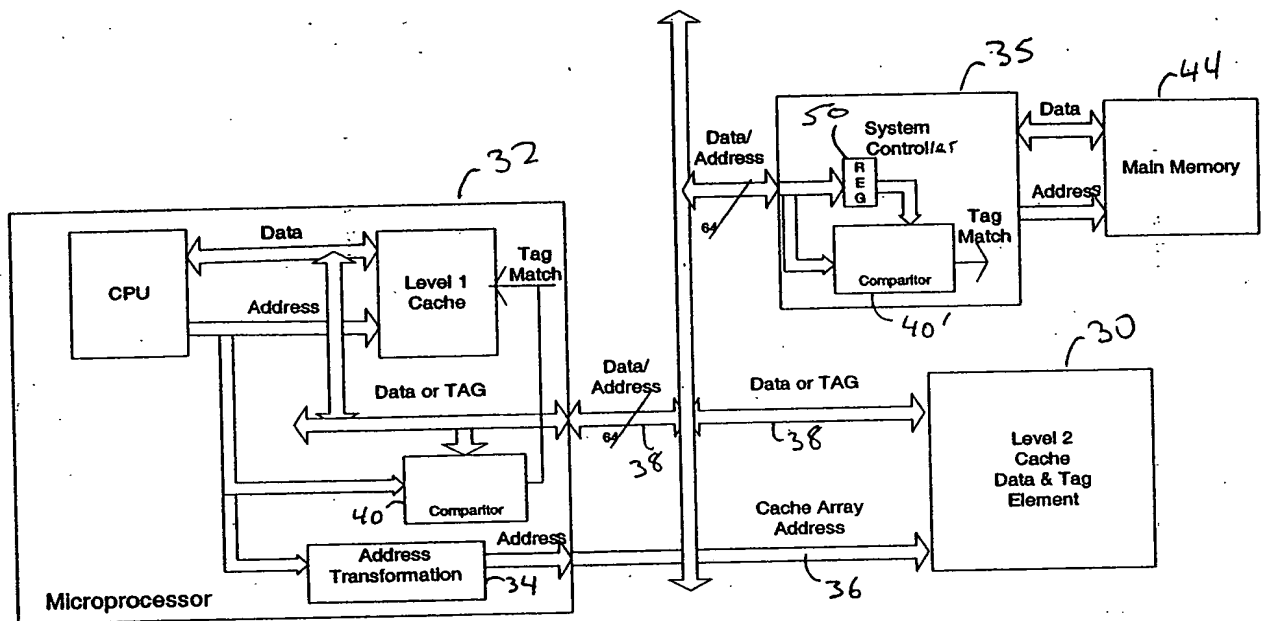
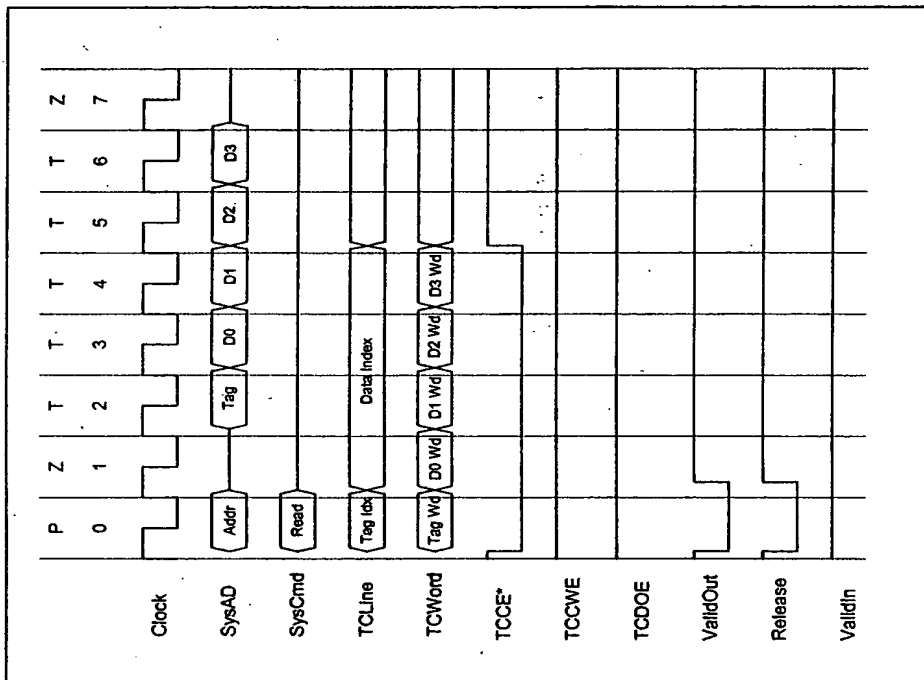


Figure 6.

MICROPROCESSOR DESIGN

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